In the Claims

Please amend claims 2-9, 11, 13-20, and 22 as set forth below. Claims 10, 12, 21, and 23 remain unchanged.

2. (Amended) A method for creating a derivative circuit design, comprising:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification analysis on the derivative circuit design.

3. (Amended) The method of claim 2, wherein the chip layout does not exceed bounds dictated by the front-end acceptance testing.

4. (Amended) The method of claim 2, further comprising the step of performing clocking and timing analysis prior to the step of performing verification analysis on the derivative circuit design.

5. (Amended) The method of claim 2, further comprising the step of performing power analysis prior to the step of performing verification analysis on the derivative circuit design.

6. (Amended) The method of claim 2, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

7. (Amended) The method of claim 2, wherein step (a) through step (e) are repeated to create a second derivative circuit design, such that the original circuit design comprises a derivative circuit design.

8. (Amended) The method of claim 2, wherein the step of planning the chip layout comprises analyzing timing requirements to ensure the derivative circuit design meets all applicable timing requirements.

9. (Amended) The method of claim 2, further comprising the step of assembling a chip based on the chip layout prior to the step of performing verification analysis on the derivative circuit design.

11. (Amended) The method of claim 10, wherein each of the one or more programmable fabrics has a port access and hierarchical routing.

13. (Amended) A computer readable medium carrying one or more sequences of one or more instructions for creating a derivative circuit design, wherein the execution of the one or more sequences of the one or more instructions causes the one or more processors to perform the steps of:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification analysis on the derivative circuit design.

14. (Amended) The computer readable medium of claim 13, wherein the chip layout does not exceed bounds dictated by the front-end acceptance testing.

15. (Amended) The computer readable medium of claim 13, further comprising the step of performing clocking and timing analysis prior to the step of performing verification analysis on the derivative circuit design.